CLAIMS

1. A sample hold circuit (14) for sampling an input potential (VG), holding the sampled potential and outputting the same, comprising:

a first switching element (15) receiving said input potential (VG) on one of its electrodes, and being turned on for a first period;

a second switching element (16) connected at one of its electrodes to the other electrode of said first switching element (15), and being turned on for a second period;

a first capacitor (19) connected at one of its electrodes to the other electrode of said second switching element (16), and receiving on the other electrode a predetermined potential (VCOM); and

a drive circuit (160) having an input node (N20) connected to the other electrode of said second switching element (16) and an output node (N30) connected to the other electrode of said first switching element (15), and providing a potential corresponding to a potential of said input node (N20) to the output node (N30).

2. The sample hold circuit according to claim 1, wherein said first and second periods are the same period.

3. The sample hold circuit according to claim 1, wherein said first period contains said second period.

4. The sample hold circuit according to claim 1, wherein said drive circuit (160) includes:

a first level shift circuit (61) providing a potential (V22) achieved by shifting a level of a potential (VI) of said input node (N20) by a predetermined first voltage in a certain direction, and

a second level shift circuit (30, 161) providing to said output node (N30) a

potential achieved by shifting a level of an output potential (V22) of said first level shift circuit (61) by a predetermined second voltage in a direction opposite to said certain potential direction.

5. The sample hold circuit according to claim 4, wherein

said first level shift circuit (61) includes:

a first current limiting element (62) receiving a first power supply potential (V3) on one of its electrodes, and

a first transistor (24) of a first conductivity type having a first electrode connected to the other electrode of said first current limiting element (62), a second electrode receiving a second power supply potential (GND) and an input electrode receiving the potential (VI) of said input node (N20); and

said second level shift circuit (30, 161) includes a second transistor (31) of a second conductivity type having a first electrode receiving a third power supply potential (V6), a second electrode connected to said output node (N30) and an input electrode connected to the other electrode of said first current limiting element (62).

6. The sample hold circuit according to claim 5, wherein

said first level shift circuit (61) further includes a third transistor (23) of a second conductivity type having a first electrode and an input electrode both connected to the other electrode of said first current limiting element (62), and having a second electrode connected to the first electrode of said first transistor (24), and

said second level shift circuit (30, 161) further includes a fourth transistor (32) of the first conductivity type having a first electrode connected to the second electrode of said second transistor (31), and having a second electrode and an input electrode both connected to said output node (N30).

7. The sample hold circuit according to claim 5, wherein

said second level shift circuit (30, 161) further includes a second current limiting element (161) connected between said output node (N30) and a line of a fourth power supply potential (GND).

8. The sample hold circuit according to claim 7, wherein

said first and second power supply potentials (V3, V6) are equal to each other, and

said second and fourth power supply potentials (GND, GND) are equal to each other.

9. The sample hold circuit according to claim 7, wherein

said first and second current limiting elements (62, 161) include first and second resistance elements, respectively.

10. The sample hold circuit according to claim 7, wherein

said first current limiting element (62) includes a third transistor (65) of the second conductivity type receiving a first constant voltage on its input electrode, and

said second current limiting element (162) includes a fourth transistor (161) of the first conductivity type receiving a second constant voltage on its input electrode.

11. The sample hold circuit according to claim 4, wherein

said drive circuit (75, 80) further includes a pulse generating circuit (76, 81) changing a potential (V22) of a predetermined node (N22) between said first and second level shift circuits (61, 30) in said certain potential direction in a pulse-like fashion in response to the change of the potential (VI) of said input node (N20) in said certain potential direction.

12. The sample hold circuit according to claim 11, wherein

said pulse generating circuit (76) includes a second capacitor (76) connected at one of its electrodes to said first node (N22), and having a potential at the other electrode being changed in said certain potential direction in a pulse-like fashion in response to the change of the potential (VI) of said input node (N20) in said certain potential direction.

13. The sample hold circuit according to claim 11, wherein

said pulse generating circuit (81) includes a third switching element (81) receiving on one of its electrodes a first power supply potential (V3), connected at the other electrode to said predetermined node (N22), and being turned on in a pulse-like fashion in response to change of the potential (VI) of said input node (N20) in said certain potential direction.

14. The sample hold circuit according to claim 4, wherein

said drive circuit (125) further includes an offset-compensating circuit (122a, S1a - S3a) canceling an offset voltage.

15. The sample hold circuit according to claim 14, wherein

the output potential of said second level shift circuit (30) is connected to a second node (N30a) instead of said output node (N121); and

said offset-compensating circuit (122a, S1a - S3a) includes:

a second capacitor (122a),

a first switching circuit (S1a, S2a) applying the potential (VI) of said input node to one of electrodes of said second capacitor (122a) and said first level shift circuit (61), and connecting the other electrode of said second capacitor (122a) to said predetermined node (N30a),

a second switching circuit (S3a) applying the potential (VI) of said input node to the other electrode of said second capacitor (122a), and applying the potential of said

one electrode of said second capacitor 122a to said first level shift circuit (61) instead of the potential (VI) of said input node, and

a third switching circuit (S4a) applying the potential of said second node (N30a) to said output node (N121).

16. The drive circuit according to claim 15, wherein

said offset-compensating circuit (122a, 126a, 131a, S1a - S3a) further includes a pulse generating circuit (126a, 131a) changing the potential of said predetermined node (N30a) in a potential direction opposite to said certain potential direction in a pulse-like fashion while said first switching circuit (S1a, S2a) is applying said input potential to one of the electrodes of said second corresponding (122a) and connection is kept between the other electrode of said second capacitor (122a) and said predetermined node (N30a).

17. The sample hold circuit according to claim 4, wherein

said drive circuit (191) further includes a switching circuit (201, 202) intermittently applying a power supply voltage to said first and second level shift circuits (21, 30).

18. An image display device comprising the sample hold circuit (14) according to claim 1; and a liquid crystal cell (2) connected at one of its electrodes to an output node (N30) of said drive circuit (20), and receiving on the other electrode a common potential (VCOM).

19. An image display device comprising the sample hold circuit (14) according to claim 1; and a liquid crystal cell (2) connected at one of its electrodes to an input node (N20) of said drive circuit (20), and receiving on the other electrode a common potential (VCOM).

20. An image display device comprising:

the sample hold circuit (226, 225, 223, 224) according to claim 1;

a transistor (222) having a first electrode connected to one of the electrodes of said first switching element (226), an input electrode connected to the other electrode of said second switching element (225), and a second electrode connected to the other electrode of said first capacitor (223);

a current supply (230) connected to the first electrode of said transistor (222) to pass a gradation current (IG) through said transistor (222) during said first and second periods of the on-state of said first and second switching elements (226, 225); and

an light-emitting element (220) connected between the first electrode of said transistor (222) and a line of a power supply potential (GND) to emit light at brightness corresponding to the current flowing through said transistor (222) after elapsing of said first and second periods.